DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5, 9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rana, U.S. Patent 5,968,188, in view of Agarwal, U.S. Patent App. Pub. 2001/0013119.

3. Referring to claim 1, Rana teaches a emulation circuit, which provides real-time code coverage data, connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a circuit for analyzing code coverage of firmware by test inputs, said circuit comprising: an input for receiving an address from a code address bus (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory, this is interpreted as a memory for storing recorded addresses form the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses

associated with the firmware (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana does not teach the contents of the memory location associated with the address received from the code address bus being incremented responsive to the receipt of the address, however Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" to determine if the code has been executed (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (See Agarwal, paragraphs 0123, 0124, and 0127). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the use of a predetermined bit pattern of the executed code of Rana with the storing of an incremented value associated with executed code of Agarwal. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for keeping count of the number of times the code has been executed (See Agarwal, paragraph 0124).

4. Referring to claim 5, Rana teaches a method of real-time code coverage with a emulation circuit connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a method for analyzing code coverage, said method comprising: receiving an address form a code address bus, the address associated with an instruction in a system on a chip (See Fig. 2, Col. 1, lines 5-

10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana does not teach incrementing a memory location mapped to the address associated with the instruction, however Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (See Agarwal, paragraphs 0123, 0124, and 0127). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the use of a predetermined bit pattern of the executed code of Rana with the storing of an incremented value associated with executed code of Agarwal. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for keeping count of the number of times the code has been executed (See Agarwal, paragraph 0124).

5. Referring to claim 9, Rana teaches a emulation circuit, which provides real-time code coverage data, connected to a target system via an address line, a data line, and a control line of a ROM socket, this is interpreted as a circuit for analyzing code coverage of firmware by test inputs, said circuit comprising: an input for receiving an

address from a code address bus (See Fig. 2, Col. 1, lines 5-10, and Col. 7, lines, lines 49-51). Rana discloses a code coverage memory comprised of multiple locations and the code coverage memory being concurrently addressed with the monitored memory, this is interpreted as a memory operably connected to the input for storing recorded addresses form the code address bus, the memory comprising a plurality of memory locations, each of the memory locations mapped to a particular one of a corresponding plurality of addresses associated with the firmware (See Fig. 2, Col. 2, line 55 to Col. 3, line 10 and Col. 5, lines 11-18).

Rana does not teach the contents of the memory location associated with the address received from the code address bus being incremented responsive to the receipt of the address, however Rana does teach the code coverage memory storing code coverage data of predetermined bit patterns that includes hexadecimal value "00" and changed to value "ff" (See Col. 8, lines 31-44). Agarwal discloses code coverage testing and flagging code that has been executed. In addition to just flagging the code that has been executed, Agarwal also teaches incrementing a value of the associated memory (See Agarwal, paragraphs 0123, 0124, and 0127). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the use of a predetermined bit pattern of the executed code of Rana with the storing of an incremented value associated with executed code of Agarwal. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for keeping count of the number of times the code has been executed (See Agarwal, paragraph 0124).

6. Referring to claim 13, Rana and Agarwal teach all the limitations (See rejection of claim 1) including incrementing the value of the associated value of memory, thereby keeping a count of the number of times the code has executed, this is interpreted as wherein the contents of the memory location associated with the address received from the code address bus are incremented responsive to receipt of the address, thereby indicating a number of times the addressed has been received (See Agarwal, paragraph 0124).

Allowable Subject Matter

7. Claims 2-4, 6-8, 10-12, and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments, see pages 4 and 5 of amendment, filed 25 July 2008, with respect to claim 15 have been fully considered and are persuasive. The objection of claim 15 has been withdrawn.

9. Applicant's arguments, see page 4 of amendment, filed 25 July 2008, with respect to claims 2, 6, and 10 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejection of claims 2-4, 6-8, 10-12, and 14-16 has been withdrawn.

10. Applicant's arguments, see pages 2-4 of amendment, filed 25 July 2008, with respect to claims 1, 5, and 9 have been fully considered but they are not persuasive. The Applicant argues that Rana and Agarwal are not combinable because the use of the incremental value of Agarwal would overwrite the predetermined bit pattern of Rana and render Rana unsatisfactory for its intended purpose. The Examiner respectfully disagrees. Rana uses one known value to indicate code that has not been executed and one known value to indicate code that has been executed. Agarwal allows for indicating that code has been executed and also how many times it has been executed. The use of the incremented value does not render the predetermined value unsatisfactory for its purpose, but rather enhances it. Therefore a first "predetermined" value is used to indicate the code has not been executed and additional "predetermined" values are used to indicate the code has been executed along with additional information indicating the number times it has been executed.

The Examiner did not rely upon the specific uses of the values of "00" and "FF" but rather that a byte value was used and therefore a 8-bit value could be used for keeping a count.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH D. MANOSKEY whose telephone number is (571)272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
October 20, 2008

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113